IN THE CLAIMS

1. (Currently Amended) A bi-directional bus circuitry shared among a plurality of circuit blocks, comprising:

a data bus divided into (J + 1) (J: natural number being 1 or more than 1) bus nodes,

each of said plurality of circuit blocks being connected to ~~any~~ one of said (J + 1) bus nodes;

a potential fixing circuit provided corresponding to one of said (J + 1) bus nodes, for setting potential level of corresponding said bus node to a prescribed potential when data is input to/output from none of said plurality of circuit blocks;

J repeater circuits provided between adjacent said bus nodes respectively,

each repeater circuit having

a first signal transmitting circuit transmitting data from one to the other of said adjacent bus nodes, and

a second signal transmitting circuit transmitting data from said the other to said one of said adjacent bus nodes; and

an arbiter circuit receiving circuit block information for specifying a circuit block which is an object of data output, and controlling activation of said first and second signal transmitting circuits,

said arbiter circuit activating, when said data is input to/output from none of said plurality of circuit blocks, either one of said first and second signal transmitting circuits in each repeater circuit, so that potential level of said bus node corresponding to said potential fixing circuit is transmitted to said data bus entirely.

2. (Original) The bi-directional bus circuitry according to claim 1, wherein

said first signal transmitting circuit includes a first tristate buffer connected in a direction from said one to said the other of said adjacent bus nodes and controlled by said arbiter circuit, and

said second signal transmitting circuit has a second tristate buffer connected in a direction from said the other to said one of said adjacent bus nodes and controlled by said arbiter circuit.

3. (Original) The bi-directional bus circuitry according to claim 1, wherein

J is 1;

said plurality of circuit blocks is divided into a first circuit block group connected to one of two bus nodes, and a second circuit block group connected to the other of said two bus nodes;

said potential fixing circuit is provided corresponding to either one of said two bus nodes;

said first signal transmitting circuit is provided for transmitting data from said one to said the other of said two bus nodes;

said second signal transmitting circuit is provided for transmitting data from said the other to said one of said two bus nodes; and

said arbiter circuit activates said first signal transmitting circuit when data is output from none of said circuit blocks belonging to said second circuit block group, and activates

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said second signal transmitting circuit when data is output from at least one of said circuit blocks belonging to said second circuit block group.

4. (Original) The bi-directional bus circuitry according to claim 1, wherein

data transmitted over said data bus has two states of high level and low level;

said potential fixing circuit includes a switch circuit connected between a power supply node supplying a potential level corresponding to either one of said high level and said low level and said corresponding bus node; and

said arbiter circuit turns on said switch circuit when said data bus is not used.

5. (Original) The bi-directional bus circuitry according to claim 4, wherein said power supply node supplies a potential level corresponding to said low level, and

said switch circuit has an N type field effect transistor.

6. (Original) The bi-directional bus circuitry according to claim 4, wherein

said power supply node supplies a potential level corresponding to said high level, and

said switch circuit has a P type field effect transistor.

7. (Original) The bi-directional bus circuitry according to claim 1, wherein

J is at least 2; and

said potential fixing circuit is provided corresponding to one of (J – 1) bus nodes among said (J + 1) bus nodes other than two bus nodes positioned at opposing ends.

8. (Original) The bi-directional bus circuitry according to claim 1, wherein

J is at least 2; and

said potential fixing circuit is provided corresponding to either one of two bus nodes positioned at opposing ends, among said (J + 1) bus nodes.

9. (Original) The bi-directional bus circuitry according to claim 8, wherein

said plurality of circuit blocks is divided into a first circuit block group connected to one of said two bus nodes positioned at the opposing ends and a second circuit block group connected to the other of said two bus nodes positioned at the opposing end; and

said first and second signal transmitting circuits in each repeater circuit are controlled by first and second control signals which are common to said J repeater circuits.

10. (Currently Amended) A bi-directional bus circuitry shared among a plurality of circuit blocks, comprising:

a data bus divided into (J + 1) (J: natural number being 1 or more than 1) bus nodes,

each of said plurality of circuit blocks being connected to ~~any~~ one of said (J + 1) bus nodes;

J repeater circuits arranged between adjacent said bus nodes,

each of said repeater circuits including

a first signal transmitting circuit transmitting data from one to the other of said adjacent bus nodes, and

a second signal transmitting circuit transmitting data from said the other to said one of said adjacent bus nodes; and

an arbiter circuit receiving circuit information for specifying a circuit block which is an object of data output, and controlling activation of said first and second signal transmitting circuits in each of said repeater circuits,

said arbiter circuit activating both of said first and second signal transmitting circuits in each of said repeater circuits when said data bus is not used, that is, when data is input to/output from none of said plurality of circuit blocks.

11. (Original) The bi-directional bus circuitry according to claim 10, wherein

said first signal transmitting circuit includes a first tristate buffer connected in a direction from said one to said the other of said adjacent bus nodes and controlled by said arbiter circuit, and

said second signal transmitting circuit has a second tristate buffer connected in a direction from said the other to said one of said adjacent bus nodes and controlled by said arbiter circuit.

12. (Original) The bi-directional bus circuitry according to claim 10, wherein

J is 1;

said plurality of circuit blocks is divided into a first circuit block group connected to one of two bus nodes, and a second circuit block group connected to the other of said two bus nodes;

said first signal transmitting circuit is provided for transmitting data from said one to said the other of said two bus nodes;

said second signal transmitting circuit is provided for transmitting data from said the other to said one of said two bus nodes; and

said arbiter circuit activates said first signal transmitting circuit when data is output from none of said circuit blocks belonging to said second circuit block group, and activates said second signal transmitting circuit when data is not output from ~~none~~ any of said circuit blocks belonging to said first circuit block group.

13. (Original) The bi-directional bus circuitry according to claim 10, wherein

J is at least 2;

said plurality of circuit blocks is divided into a first circuit block group connected to one of two bus nodes positioned at opposing ends, and a second circuit block group connected to the other of said two bus nodes;

said first signal transmitting circuit in each repeater circuit is provided for transmitting data in a direction from said one to said the other of said two bus nodes;

said second signal transmitting circuit in each repeater circuit is provided for transmitting data in a direction from said the other to said one of said two bus nodes;

said first and second signal transmitting circuits in each repeater circuit are controlled by first and second control signals provided commonly to said J repeater circuits; and

said arbiter circuit activates said first signal transmitting circuit in each repeater circuit when data is output from none of said circuit blocks belonging to said second circuit

block group, and activates said second signal transmitting circuit in each repeater circuit when data is output from none of said circuit blocks belonging to said first circuit block group.